GPU accelerated SoCs as Flight Computers for Small Satellites

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Overview

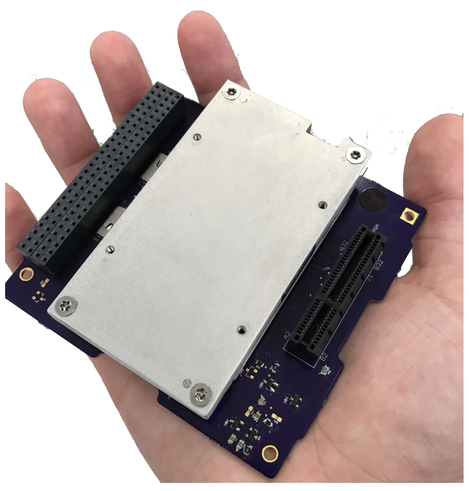

Figure 1: First Iteration Accelerated Flight Computer Core GPU Interface (CORGI)

The University of Georgia's Small Satellite Research Laboratory (SSRL) is utilizing a Nvidia TX2i Graphics Processing Unit (GPU) within the Multi-view Onboard Computational Imager (MOCI) Satellite. Although the system utilizes a GPU an additional On Board Computer (OBC) is still required for control and communication with core avionics. The UGA SSRL has developed a board, the Core GPU Interface (CORGI), that is capable of interfacing the Nvidia TX1, Nvidia TX2, or Nvidia TX2i into a PC104+ compliant CubeSat [1][2][3]. In this paper we discuss the previously designed CORGI board and elaborate on lessons learned, including how the CORGI is being used to combine an OBC and an Nvidia TX2i into one board. We call this new board, that is still undergoing development, the Accelerated Flight Computer (AFC).

Form Factor

The CubeSat form factor is the primary driver in the design of the AFC. The form factor complies with available Poly Picosatellite Orbital deployers (P-POD), general NanoRacks specifications, and is modular to adapt to changes in payload and support I/O both spatially and functionally [10][11] The CORGI (See Figure 1) board provided a design benchmark satisfying mission and development requirements for the MOCI mission, but didn't offer the payload capability of an accelerated heterogeneous. The CORGI currently uses b i-directional logic shifters to match up its 1.8V (CMOS). The SF2 ARM Cortex allows integration of an embedded flash based FPGA, and the Jetson. The SF2 ARM Cortex allows integration of an embedded flash based FPGA, and the JetsonTX2/TX2i module in a compact design (50 mm x 87 mm). A 400-pin compatible board-to-board connector will also interface with the TX2i module via a 8x50 connector (SEAM-50-02.0-S-08-2-A-K-TR).

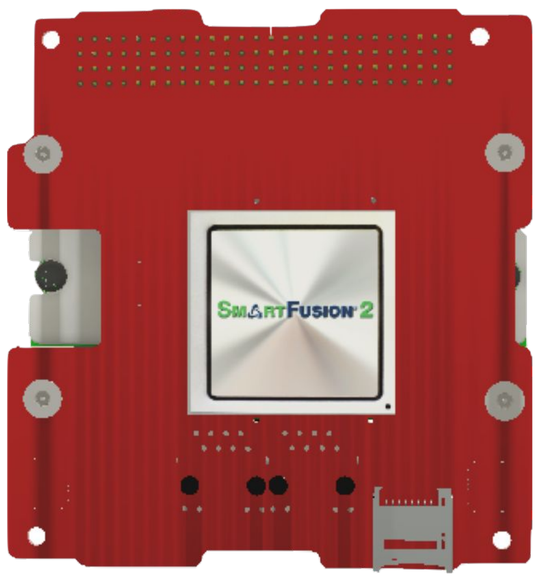

Figure 2: Back of Accelerated Flight Computer

Architecture

With ubiquitous computing and 10/100/1000 Ethernet Switching, Ethernet provides wired communication for the satellite bulk data transfer between the SF2 and TX2i. This design contains carrier level Ethernet whose data link and physical layer protocol are described by the IEEE 802.3.[14] This design utilizes a node switch which acts as a physical medium. This protocol has built in collision prevention providing full duplex comparable to that of a point to point topology, thus GPU-GPU and CPU-GPU communications can be accomplished without garbling data. Being the primary distributer of the workload the design contains the SF2 with SEU Protected/Tolerant Memories i.e: eSRAMs, DDR3.programmable gate array (FPGA) microcontroller subsystem (MSS)

The MSS includes a watchdog a which provides the bare metal system with no operating system to detect and respond to lockups caused by heavy ion bombardment [13]. This is described in more detail in the radiation and thermal mitigation section. The SF2 will utilize 4 x 256 DDR3 (MT41K256M8DA-125 IT:K) external memory banks providing volatile memory. In addition the

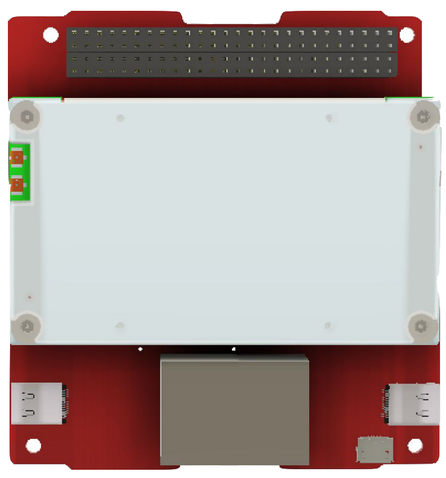

Figure 3: Front of Accelerated Flight Computer

TX2i's and SF2 share RAD NOR SPI flash memory (Cypress CYRS16B256).The SF2 will allow mediated read/write access with the purpose of sharing mutually relevant files. This functionality is defined in hardware via MUX whose selection is determine by GPIO pins from SF2 SOC, active high.

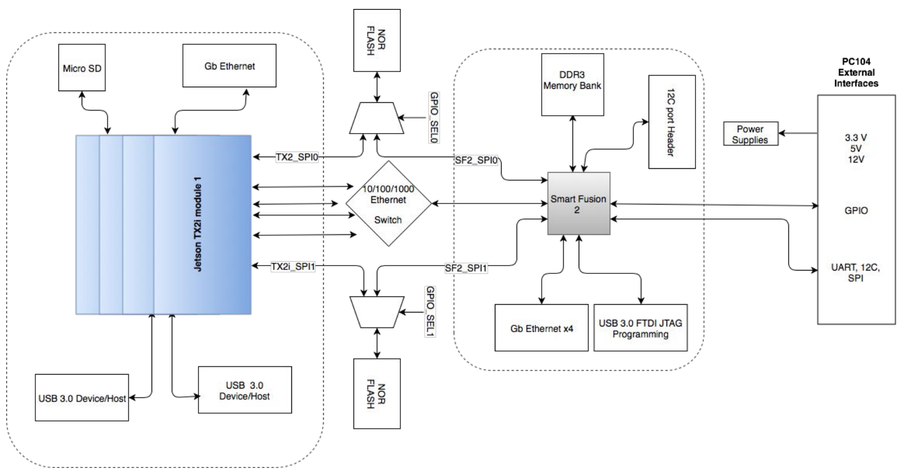

Figure 4: AFC Hardware Architecture

These interfaces will be a Gb Ethernet local network, and shared flash memory that the Smart Fusion 2 and TX2i's will access via multiplexed SPI connections. The ethernet line will be used by the Smart Fusion 2 to distribute computation tasks and the data those computations will be performed on to the TX2i's. These ethernet communications will take the form of multicast messages for things that each TX2i will need to receive and direct messages for communication to individual TX2i's. The computation tasks to be distributed to each TX2i will take the form of CUDA code that will instruct each gpu what computations it should carry out on which data. The TX2i's will make use of the ethernet line to kick the watchdogs (see software radiation mitigation section) on the Smart Fusion 2 and to log their progress or telemetry back to the Smart Fusion 2. The Smart Fusion 2 will use the SPI accessed shared flash memory as it's primary persistent memory where it will store logged telemetry as well as tasks and data to distribute to the TX2i's.The TX2i's will make use of the shared flash memory by writing the output of their computations to it. In order for that to happen the Smart Fusion 2 will have to make use of the ethernet line to tell the TX2i's what to write, where to write, and when to write to shared memory.

Thermal Analysis

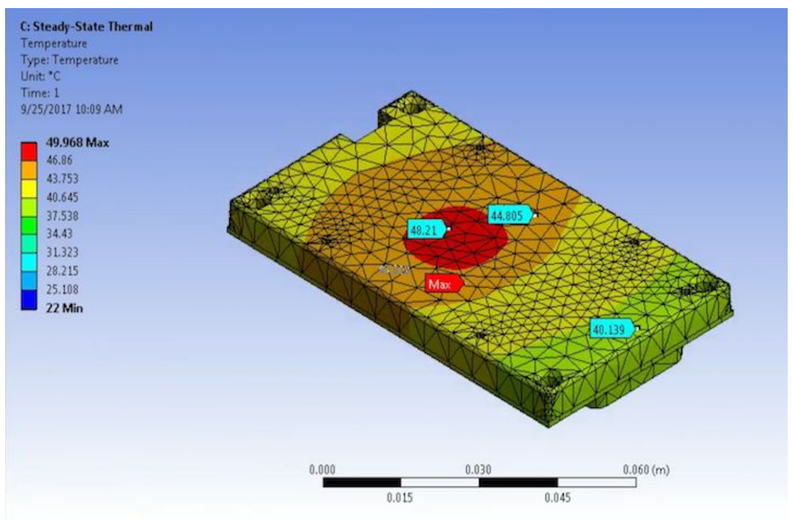

Figure 5: Thermal Simulation for Tegra TX2

Radiation mitigation in LEO we recommend utilizing the Dunmore Aerospace “Satkit” which contains the standard STARcrest MLI materials cut into manageable sizes for small satellite developers allowing them to develop their own thermal protection blankets for LEO protection. The kit includes an outer Layer material, inner Layer material, first surface tape, and clear polyimide tape[15]. This kit is optimal for small satellite systems, as it is small, cheap, and easily customizable. More specifications of the materials are listed below in (See Figure 4) and values were calculated from the Solar Radiation, Earth’s IR radiation, and Albedo Radiation equations [16].

Future Work

- (Paralleled Thread Execution) PTX assembly to checkpoint GPU operations.
- Test Network with multiple TX2is
- Vacuum Chamber testing i.e: CVCM, TML.
- FlatSat integration testing with satellite peripherals.

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